|  |
| --- |
| **Computer Architecture**   * Refers to those attributes of a system visible to a programmer or those attributes that have direct impact on the logical execution of a program. A term that is interchangeably used with computer architecture is **instruction set architecture (ISA).** * ISA defines   + instruction formats   + instruction opcodes   + instruction and data memory   + The effect of executed instructions on registers and memory   + An algorithm for controlling instruction execution.   **Computer Organization**   * Refers to those hardware details transparent to the programmer * Such as   + Control signals   + Interfaces between computer and peripherals   + Memory technology used   For example, it is an architectural design issue whether a computer will have  a multiply instruction. It is an organizational issue whether that instruction will be  implemented by a special multiply unit or by a mechanism that makes repeated  use of the add unit of the system. |
| The most primitive operations that can be performed on data are   * Data processing * Data storage * Data movement (Communication) * Control |
| |  |  |  |  |  | | --- | --- | --- | --- | --- | | |  |  | | --- | --- | | **Instruction Set Architecture** | **Micro-architecture** | | * Interface between software and hardware. Software and compiler assumptions. Hardware promises. What the software writer needs to know and debug the system and user programs | * Implementation of ISA. The fundamental design of micro-processor. Abbreviated as uArch. It is not visible to the software. | | | **Advantages of using IP**  Control driven, Sequential execution. Offer precise location and state easy to debug as opposed to Data flow Model Easy. Overall cost is lower  **Disadvantages of using IP**  Limited instruction execution speed. Requires more time to complete a task. More suitable for single threaded applications. More suitable when there is a single processor.  **Advantages of using Dataflow model**  Data driven, parallel execution. Lowers the process execution time significantly by exploiting more than one processors giving higher performance.  **Disadvantages of Dataflow model**  Makes it difficult to write and debug the program. A relatively simple program that is much easy to write in sequential order, makes it difficult to understand when implementd in dataflow model. | |
|  |
| When interrupts are enabled, processor continously checks for interrupts after each instruction execution. When interrupt cycle is added in the fetch-decode-execute cycle, no interrupt goes unseen.   * If no interrupt, fetch next instruction * If interrupt pending: Suspend execution of current program Save context Set PC to start address of interrupt handler routine Process interrupt Restore context and continue interrupted program. |
|  |
|  |
|  |
|  |
|  |
|  |